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ORIGINAL PAPER

The Connectivity and Diameter of Second Order Circuit Graphs of Matroids

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Abstract Let $C_2(M)$ be the second order circuit graph of a simple connected matroid M, then $C_2(M)$ is 2-connected if M has more than one circuit and M is not a line. Moreover, $C_2(M)$ has diameter at most two if and only if M does not have any restriction isomorphic to $U_{2,6}$.

Keywords Matroid · Circuit graph of a matroid · Second order circuit graph of a matroid · Connectivity · Diameter

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1 Introduction

Matroids and graphs considered in this paper are finite. We follow the notations and terminology in [2] for graphs and [15] for matroids except otherwise defined. Let M

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be a matroid on a set E. The *corank* $r^*(M)$ of a matroid M is the rank of M^*, the dual of M. For a subset $S \subseteq E$, we abbreviate the expression $r^*(M|S)$ as r^*S, and the *dimension* dS of S is defined to be the number $r^*S - 1$. Following Tutte [15], a subset S of E is called a *flat* of M if it is a union of circuits of M. The null subset of E is considered as a null union of circuits, and therefore a flat. Note that our definition of a flat here is different from that in [14].

For any subset S of E there is an associated flat $\langle S\rangle$, defined as the union of all the circuits of M contained in S. Thus $\langle S\rangle$ is the union of the circuits of $M|S$. Note that $d\langle Z\rangle = dZ = r^*Z - 1$. A flat S is *on* a flat T if either $S \subseteq T$ or $T \subseteq S$. A flat of dimension k is called a *k-flat*. The 1-flats and 2-flats of M are the *lines* and the *planes* of M, respectively. A flat S of M is called *connected* if $M|S$ is a connected matroid.

There have been many studies on the properties of graphs arising from matroids. In [15], Tutte defined the *circuit graph* of a matroid M, denoted by $C(M)$, whose vertices are the circuits of M, where the two vertices in $C(M)$ are adjacent if and only if they are distinct circuits of the same connected line. Tutte [15] showed that a matroid M is connected if and only if $C(M)$ is a connected graph. In [12,13], Maurer defined the base graph of a matroid. The vertices are the bases of M and two vertices are adjacent if and only if the symmetric difference of these two bases is of cardinality 2. He also discussed the graphical properties of the base graph of a matroid. Alspach and Liu [1] studied the properties of paths and circuits in base graphs of matroids. The connectivity of the base graph of matroids is investigated by Liu in [9,10]. The graphical properties of the matroid base graphs have also been investigated by many other researchers, see [3–5,11], among others.

Recent studies by Li and Liu [6–8] initiate the investigation of graphical properties of matroid circuits graphs. Let M be a matroid, and let $k > 0$ be an integer. The *kth order circuit graph* $C_k(M)$ of M has vertex set $V(C_k(M)) = \mathcal{C}(M)$, the set of all circuits of M. Two vertices $C, C' \in \mathcal{C}(M)$ are adjacent in $C_k(M)$ if and only if $|C \cap C'| \geq k$. For notational convenience, for a circuit $C \in \mathcal{C}(M)$, we shall use C to denote both a vertex in $C_k(M)$ and a circuit (also as a subset of $E(M)$) of M.

In their studies [6–8], Li and Liu proved that $C_1(M)$ possesses quite good graphical connectivity properties. The purpose of this paper is to investigate the graphical properties possessed by $C_2(M)$, a spanning subgraph of $C_1(M)$, which represents a relatively loose interrelationship among circuits in the matroid. We have proved in this paper that for a connected simple matroid M, the diameter of $C_2(M)$ is at most 2 if and only if M does not have a restriction isomorphic to $U_{2,6}$. Moreover, if a connected simple matroid M is not a line, then $C_2(M)$ is 2-connected.

In Sect. 2, we shall review some former results and develop certain useful lemmas what will be needed in this paper. The last section will be devoted to the proofs of the main results.

2 Useful Results on Circuits and Flats

In this section, we summarize some of the useful former results, and developed a few lemmas for our use. A matroid M is trivial if it has no circuits. In the following all matroids will be nontrivial.

Theorem 1 (Tutte [15]) *Let M be a matroid.*

(i) (Theorem 4.21 [15]). *Let L be a line of M and $a \in L$, then $\langle L - \{a\}\rangle$ is the only circuit on L which does not include a.*

(ii) (Theorem 4.28 [15]). *Let L be a disconnected line on a connected d-flat S of M, where $dS > 1$. Then there exists a connected plane P of M such that $L \subset P \subseteq S$.*

(iii) (Theorem 4.281 [15]). *Let L be a disconnected line on a plane P of M. Let X and Y be its two circuits, and let Z be any other circuit on P. Then $X \cup Z$ and $Y \cup Z$ are connected lines, the only lines of M which are on both Z and P.*

(iv) (Theorem 4.36 [15]). *A matroid M without coloops is connected if and only if its circuit graph $C(M)$ is a connected graph.*

Also, throughout the rest of this section, M denotes a simple nontrivial matroid, and C_1 and C_2 will denote two distinct circuits of M.

Lemma 1 *If C_1 and C_2 are different circuits of a matroid M such that $C_1 \cap C_2 = \{e\}$, then:*

(i) *If C_1 and C_2 are on a line, then $C_1 \triangle C_2$ is a circuit of M and $|(C_1 \triangle C_2) \cap C_i| \geq 2$.*

(ii) *If C_1 and C_2 are not on a line, then there are circuits C_3 and C_4 of M such that $e \in C_3 \cap C_4$, C_1, C_2, C_3, C_4 are pairwise different and $|C_i \cap C_j| \geq 2$, for every $i \in \{1, 2\}$ and $j \in \{3, 4\}$.*

Proof First, we establish (i). Observe that $C_1 - C_2$ and $C_2 - C_1$ are series classes of $M|(C_1 \cup C_2)$. Since $M|(C_1 \cup C_2)$ is connected, for each element $e' \in C_1 \triangle C_2$ there is a circuit C of M such that $e' \in C \subseteq C_1 \triangle C_2 = (C_1 - C_2) \cup (C_2 - C_1)$. By Theorem 1 (i), C is the only circuit on $\langle C_1 \triangle C_2\rangle$. Therefore $C_1 \triangle C_2 = (C_1 \cup C_2) - e \subseteq C$, and so $C_1 \triangle C_2$ is a circuit of M.

To prove (ii), let L be a connected line of M such that $C_1 \subseteq L \subseteq C_1 \cup C_2$. Choose a circuit C_3 of M such that $e \in C_3 \subseteq L$ and $C_3 \neq C_1$. There is a connected line L' of M such that $C_2 \subseteq L' \subseteq C_1 \cup C_2$ and $\langle L' \cap C_3\rangle = \emptyset$. We can choose a circuit C_4 of M such that $e \in C_4 \subseteq L'$ and $C_4 \neq C_2$. □

Lemma 2 *If C_1 and C_2 are on a disconnected line of a connected matroid M, then there is a circuit C_0 such that $C_1 \cup C_0$ and $C_2 \cup C_0$ are connected lines with $|C_1 \cap C_0| \geq 2$ and $|C_2 \cap C_0| \geq 2$.*

Proof By assumption, $M|(C_1 \cup C_2)$ is a disconnected line. Since M is connected, by Theorem 1(ii), there exists a connected plane P of M such that $C_1 \cup C_2 \subset P$. By Theorem 1(iii), let C be any other circuit on P, then $C_1 \cup C$ and $C_2 \cup C$ are connected lines. Assume that there is not a circuit C_0 on P such that $|C_1 \cap C_0| \geq 2$ and $|C_2 \cap C_0| \geq 2$. By Lemma 1, we know that there is a circuit C_3 with $|C_1 \cap C_3| \geq 2$. Then $|C_2 \cap C_3| = 1$. By Lemma 1, $C_2 \triangle C_3$ is a circuit and $|(C_2 \triangle C_3) \cap C_2| \geq 2$. But also $|(C_2 \triangle C_3) \cap C_1| \geq 2$, a contradiction. □

Lemma 3 *Let C_1 be a circuit of M. If $e \notin C_1$, then there is a circuit C_2 containing e and C_1 and C_2 are on a connected line.*

Proof Since M is connected, there is a circuit C' containing e and $|C_1 \cap C'| \neq 0$. Let C_2 be such a circuit and $|C_1 \cup C_2| - r(C_1 \cup C_2)$ is minimal. Since M is binary, $C_1 \triangle C_2$ is a disjoint union of circuits of M. If $C_1 \triangle C_2$ is a circuit, then C_1 and C_2 are on a connected line. If $C_1 \triangle C_2$ is not a circuit, then there is $C_3 \subset C_1 \triangle C_2$ containing e. So we have $|C_1 \cup C_3| - r(C_1 \cup C_3) < |C_1 \cup C_2| - r(C_1 \cup C_2)$ which is a contradiction. So C_1 and C_2 are on a connected line. □

Lemma 4 *If $|C_1 \cap C_2| = 0$, and $r(C_1) < r(C_1 \cup C_2) < |C_1 \cup C_2| - 2$, then there is a circuit C in $M|(C_1 \cup C_2)$ such that C and C_1 are on a connected line with $|C_1 \cap C| \geq 2$, $|C_2 \cap C| \geq 2$.*

Proof There is $e \in C_2$ such that C_1 does not span e because, by hypothesis, $r(C_1) < r(C_1 \cup C_2)$. By Lemma 3, there is a connected line L such that $C_1 \cup e \subseteq L \subseteq C_1 \cup C_2$. If C is a circuit of M such that $e \in C \subseteq L$ and $C \neq C_1$, then $L - C_1 \subseteq C$ and so $|C \cap C_2| \geq 2$. Since $|C_1| \geq 3$, it is possible to choose C such that $|C \cap C_1| \geq 2$.

□

3 Main Results

In this section, we shall prove our main results.

Theorem 2 *Let M be a connected simple matroid with more than one circuit. The following statements are equivalent:*

(i) *M does not have a restriction isomorphic to $U_{2,6}$.*

(ii) *$diam(C_2(M)) \leq 2$.*

Proof Assume that (i) holds. Let C_1 and C_2 be two circuits of M. We shall show that in $C_2(M)$, either C_1 and C_2 are adjacent, or there is a C_3 which is adjacent to both C_1 and C_2. Since if $|C_1 \cap C_2| \geq 2$, then C_1 and C_2 are adjacent in $C_2(M)$, we assume that $|C_1 \cap C_2| \leq 1$.

Note that if $C_1 \cap C_2 = \{e\}$, then (ii) follows from Lemma 1. Hence we may assume $|C_1 \cap C_2| = 0$. In this case, we have $r(C_1 \cup C_2) \leq |C_1 \cup C_2| - 2$.

Case 1. If $r(C_1 \cup C_2) = |C_1 \cup C_2| - 2$, then $M|(C_1 \cup C_2)$ is a disconnected line. By Lemma 2, we can find a circuit C_0 such that $C_1 \cup C_0$ and $C_2 \cup C_0$ are connected lines with $|C_1 \cap C_0| \geq 2$ and $|C_2 \cap C_0| \geq 2$.

Case 2. If $r(C_1 \cup C_2) < |C_1 \cup C_2| - 2$, then $M|(C_1 \cup C_2)$ is connected. If $r(C_1 \cup C_2) > r(C_1)$ or $r(C_1 \cup C_2) > r(C_2)$, without loss of generality, we assume that $r(C_1 \cup C_2) > r(C_1)$. By Lemma 4, there is a circuit C_0 in $M|(C_1 \cup C_2)$ such that C_0 and C_1 are on a connected line and $|C_1 \cap C_0| \geq 2$, $|C_2 \cap C_0| \geq 2$.

Case 3. If $r(C_1 \cup C_2) < |C_1 \cup C_2| - 2$ and $r(C_1 \cup C_2) = r(C_1) = r(C_2)$, assume that in $C_2(M)$, C_1 and C_2 do not have a common adjacent vertex. Since M is a simple matroid, then $|C_2| \geq 3$. Hence there are elements $f_1, f_2, f_3 \in C_2$ and $f_i \neq f_j$ for any $i \neq j$ $(i, j = 1, 2, 3)$.

Subcase 3.1. $\{f_1, f_2, f_3\} = C_2$. Then $r(C_1 \cup C_2) = r(C_1) = r(C_2) = 2$. Therefore $M|(C_1 \cup C_2)$ is isomorphic to $U_{2,6}$ which is a contradiction.

Subcase 3.2. $\{f_1, f_2, f_3\} \subset C_2$. Therefore in $M|(C_1 \cup \{f_i, f_j\})$, any circuit containing f_i and f_j has length 3 ($i \neq j, i, j = 1, 2, 3$). Hence we can find a circuit $C_3 = \{f_1, f_2, h\}$ and $C_4 = \{f_2, f_3, g\}$ such that $h, g \in C_1$. Since $r(\{f_1, f_2, f_3\}) = 3$, by Lemma 1, $\{f_1, h, f_3, g\}$ is a circuit of M. Then we can get a vertex adjacent to both C_1 and C_2 which is also a contradiction.

Conversely, if M has a restriction X isomorphic to $U_{2,6}$, let C_1 and C_2 be two different circuits of X and $C_1 \cap C_2 = \emptyset$, then the distance between C_1 and C_2 in $C_2(M)$ is 3. If not, then we have a circuit C' of M with $|C' \cap C_1| \geq 2$ and $|C' \cap C_2| \geq 2$. Let $Y = (C' \cap C_1) \cup (C' \cap C_2)$. Then $|Y| \geq 4$ and $Y \subseteq X$. Since $M|X \cong U_{2,6}$, and since $|Y| \geq 4$, Y must properly contain a circuit of M, contrary to the circuit axioms.

This completes the proof of the theorem. □

Theorem 3 *Let M be a connected simple matroid with more than one circuit, but M is not a line, then $C_2(M)$ is 2-connected.*

Proof We argue by contradiction, and assume that $C_2(M)$ has a cut vertex C_0. Let C_1 and C_2 be circuits of M such that they are in two different components of $C_2(M) - C_0$ and $|C_1 \cap C_2| = 1$. By Lemma 1(ii), C_1 and C_2 are on a connected line. By Lemma 1(i), $C_0 = C_1 \triangle C_2$. As M is not a line, there is another circuit C_3 in different components of $C_2(M) - C_0$ with C_i and $|C_3 \cap C_i| = 1$ ($i = 1$ or 2). Without loss of generality, we assume that $|C_3 \cap C_1| = 1$. By Lemma 1, C_1 and C_3 are both adjacent to $C_1 \triangle C_3$ which is also a circuit of M. Therefore, $C_2(M)$ has a path joining C_1 and C_2 without passing through C_0, contrary to the assumption that C_0 is a cut vertex of $C_2(M)$ separating C_1 and C_2. This contradiction establishes the theorem. □

We conclude the paper with the following result on the connectivity of $C_k(M)$.

Theorem 4 *If M is a connected matroid with girth at least $2k - 1$, then $C_k(M)$ is connected.*

Proof Let CD be an edge of $C(M)$. By definition, C and D are different circuits of a connected line of M. If $|C \cap D| \geq k$, then CD is an edge of $C_k(M)$. If $|C \cap D| < k$, then $C \triangle D \subseteq C'$, for some circuit C' of M. Since $|C \cap C'| \geq |C - D| \geq (2k-1) - (k-1) = k$, CC' is an edge of $C_k(M)$. Similarly, DC' is also an edge of $C_k(M)$. Therefore if C and C are circuits of M and if C and D are adjacent in $C(M)$, then C and D are joined by a path of length at most 2 in $C_k(M)$. Since $C(M)$ is connected, $C_k(M)$ is also connected. □

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